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CARL S. DOBBS

SUMMARY OF QUALIFICATIONS

More than 20 years business and technical experience in IC design and development with extremely broad and deep knowledge of the IC design process, the tools, and flow. Span of knowledge is from transistor level design, layout, and verification through logic design and synthesis up to micro-architecture and system level specification. Tool knowledge spans from tool specification and development through integration and flow up to administration of the computer systems required to run them. Process participation experience spans from technical contribution through the founding, growth, and sale of multiple companies.

PROFESSIONAL EXPERIENCE

2004 - Date Fourteen Consulting Austin, TX

Founder, CEO, & Principal Consultant

- Founded Fourteen Consulting to provide both technical and business consulting services in the silicon IC design and EDA tool areas.
- Consulted with several early stage startups along with assisting with due diligence efforts for early investors.
- Currently performing technical consulting on the physical implementation of a 5 Million gate ASIC in the networking space. Focus is on the development of a robust flow and the design efforts required for synthesis, formal verification, timing analysis, and placement for a structured ASIC implementation. Also participated in the development and bring-up of an FPGA version of the design.

2000 - 2004 Synopsys, Inc. Austin, TX

SPS Design Flow (TIGER) Technical Manager

- Primary focus was on the technical leadership and management of the TIGER flow development for Synopsys Professional Services (SPS). Helped lead cross-functional team of designers in development of a flow and methodology for use in all of SPS. In addition, led collaboration with IC Implementation Business Unit (a tool development group) to help in flow standardization across entire corporation. Full Spec to GDSII flow was developed and released. Technical responsibilities included system architecture, interface development, script specification and development, documentation, training development and delivery, infrastructure interfacing, regression testing, automation, inter- and intra- team communication, and progress tracking and reporting.
- Developed and delivered training to three sites in Europe as well as three sites in US.
- Acted as technical consultant on several projects and as mentor for less experienced designers.

- Directly delivered design consulting services on several projects.
- Working in collaboration with other designers, developed many templates and documents to help in all aspects of the design process.
- Instrumental in development of both the TIGER website and the content on the SPS website.
- Participated in many early customer engagement and development activities.
- Representative to SPS Engineering Council.
- Participated in Synopsys corporate flow/methodology summit held by Chi-Foon Chan, Feb 2001.
- Member of committee to define and direct SPS usage of DSA technology.
- Assisted in marketing collateral development.
- Lead technical contributor for Synopsys in the development of the Soft IP Tagging Standard for the VSI Alliance.

1992 - 2000 The Silicon Group, Inc. Austin, TX

Founder, CEO, & Principal Designer

- Instrumental in negotiation and sale of the Silicon Group, Inc, to Synopsys, Inc. in 2000.
- Assisted business plan development, management and policy setting.
- Management and oversight of over fifty designs including full chips, individual modules, and FPGAs. Process technologies ranged from 0.8um to 0.18um CMOS. Operational frequency on projects ranged from 20 MHz up to 500 MHz. Direct design responsibilities on over fifteen of these projects.
- Design responsibilities included design tool selection, flow development, tool integrations, technology selection and insertion, specification development, RTL development, simulation, micro-architecture, logic synthesis, custom logic design, circuit design and simulation, manual and automated layout, extraction, timing analysis, logical and physical design verification, test development, and design debug and enhancement.
- Other responsibilities included facilities planning and management, computer system administration, contract management, and business development.
- Member of Technical Advisory Board for early stage EDA company, Real Intent 1999 – 2001.

1988 - 1992 ROSS Technology, Inc. Austin, TX

Founder, Vice President, Director of Design, Director of CAD

- Participated in overall corporate management, including business plan development, stock plan administration, MIS management, facilities development and direction, and design and CAD team management.
- As Director of CAD responsibilities included all aspects of design support including the workstation network; design tool selection, integration, support, and development; layout generator development; and cell and block level design and verification for all design projects including the ROSS HyperSPARC processors.

- As Director of Design duties included management, oversight of the design, and design contribution on two SPARC cache controller and memory management unit chips. Both chips included embedded memory, custom datapath, and custom control logic.
- Design responsibilities included micro-architecture specification, functional modeling, logic design, transistor level circuit design, all simulation, test vector development, layout generator development, design verification, mask generation, and post tape-out yield enhancement.

1985 - 1988 Motorola, Inc. Austin, TX

Circuit Design Manager – SPS – Advanced Microprocessor Operations

- Led implementation (RTL through layout) team that took 88100 32-bit RISC processor from concept to production.
- Specific areas of responsibility and expertise included: micro-architecture, modeling, simulation, logic, circuits, layout, verification, mask prep, package design, test development, interface to fab and product test.
- Manager of RISC hardware and software design / development lab.
- Member Motorola Technical Ladder

1984 - 1985 Motorola, Inc. Austin, TX

CMOS Standard Cell Design Engineer – SPS - ASIC Division

- Developed initial Motorola standard cell design flow and design manual.
- Coordinated multiple design centers.
- Developed automated power bussing specifications and algorithms.
- Developed and characterized standard cell I/O buffer families and test chips.

1982 - 1984 Texas Instruments, Inc. Houston, TX

Circuit Design Engineer – Custom Components Division

- Project leader in development of procedural PLA generator.
- Performed design, layout, and verification of standard cell library and implemented customer designs in first TI CMOS standard cell products.

Summer 1981
Summer 1980 Sandia National Laboratories Albuquerque, NM

Engineering Internship

- Developed test system and obtained data for characterization of Metal-Nitride-Oxide-Semiconductor (MNOS) memory devices.

EDUCATION

1980 - 1982 University of Arkansas Fayetteville, AR

MSEE

- Thesis – "Charge Loss in Metal-Nitride-Oxide-Semiconductor (MNOS) Devices at High Temperatures"
- GPA 4.0/4.0

1975 - 1980 University of Arkansas Fayetteville, AR

BSEE

- Co-operative education option provided four (4) semesters of work experience in telecom consulting with Aubrey Carroll Company in Little Rock, AR.
- GPA 4.0/4.0

PATENTS

Pat. No. 5,933,594 "Diagnostic System for Run-time Monitoring of Computer Operations"

Pat. No. 5,630,048 "Diagnostic System for Run-time Monitoring of Computer Operations"

Pat. No. 5,173,617 "Digital Phase Lock Clock Generator without Local Oscillator"

PUBLICATIONS AND CONFERENCES

"Virtual Component Identification Soft IP Tagging Standard", VSI Alliance, (one of several contributors), August 2004

"Design Outsourcing: Here Today, Here to Stay", Panel Discussion: "Outsourcing Design: Blessing or Curse?" - Custom Integrated Circuits Conference, May 2000

"Custom IC Design Methodology for HyperSPARC", Asia-Pacific Design Seminar presented by Mentor Graphics Corp., Sep 1992

"Smaller is Better", DAC Executive Forum – "Thriving on Change", 28th Design Automation Conference, Jun 1991

"Supercomputing on Chip: Genesis of the 88000", VLSI Systems Design, May 1988

"IC Design Tools Required Within the Changing Design Environment", Automated Design and Engineering for Electronics Conference, Mar 1986

"Charge Loss in Metal-Nitride-Oxide-Semiconductor (MNOS) Devices at High Temperatures", Solid-State Electronics, Vol. 26, No. 5, 1983

ADDITIONAL PROFESSIONAL ACTIVITIES

Mentor, The Capital Network, 2002, TCN worked with select growth companies to help them prepare for and target appropriate sources of capital

Real Intent, Inc. (Formerly Validity Design Automation) Technical Advisory Board member, Feb 1999 – Dec 2001

Arkansas Academy of Electrical Engineers, Member since 2000, An honorary society (limited to 125 alumni) to recognize outstanding graduates of the University of Arkansas with more than 20 years of distinguished contribution to the field of Electrical Engineering

PROFESSIONAL MEMBERSHIPS

Tau Beta Pi, Eta Kappa Nu, IEEE

COMMUNITY ACTIVITIES

Member Parish Council of Emmaus Catholic Church in Lakeway, Texas, 2004 – present

City of Lakeway Board of Ethics Member (appointed volunteer), 1998-2002, Secretary 1999-2002

PERSONAL

Married with two children

HOBBIES

Computers, gaming, electronics, reading, softball, woodworking, music, construction, exercise